19-1597; Rev 0; 1/00

10-Bit, 20Msps ADC

General Description

The MAX1425 10-bit, monolithic analog-to-digital converter (ADC) is capable of a 20Msps sampling rate. This device features an internal track-and-hold (T/H) amplifier for excellent dynamic performance; at the same time, it minimizes the number of external components. Low input capacitance of only 8pF minimizes input drive requirements. A wide input bandwidth (up to 150MHz) makes this device suitable for digital RF/IF downconverter applications employing undersampling techniques.

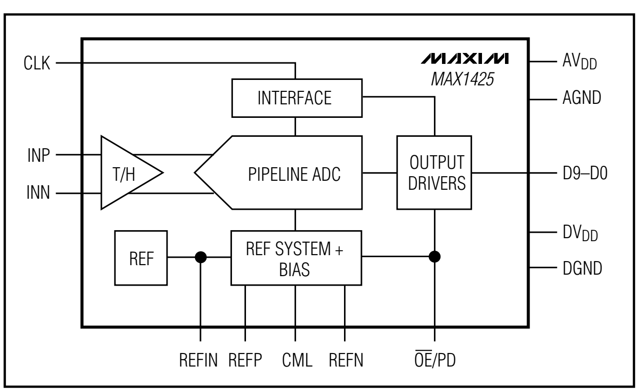
The MAX1425 employs a differential pipelined architecture with a wideband T/H amplifier to maximize throughput while limiting power consumption to only 172mW. The MAX1425 generates an internal +2.5V reference that supplies three additional reference voltages (+3.25V, +2.25V, and +1.25V). These reference voltages provide a differential input range of +2V to -2V. The analog inputs are biased internally to correct the DC level, eliminating the need for external biasing on AC-coupled applications.

A separate +3V digital logic supply input allows for separation of digital and analog circuitry. The output data is in two's complement format. The MAX1425 is available in the space-saving 28-pin SSOP package. For a pin-compatible version at a lower data rate, refer to the MAX1426 data sheet. For a higher data rate, refer to the MAX1424 data sheet.

Applications

- Medical Ultrasound Imaging
- CCD Pixel Processing
- IR Focal Plane Array
- Radar
- IF and Baseband Digitization
- Set-Top Boxes

Functional Diagram



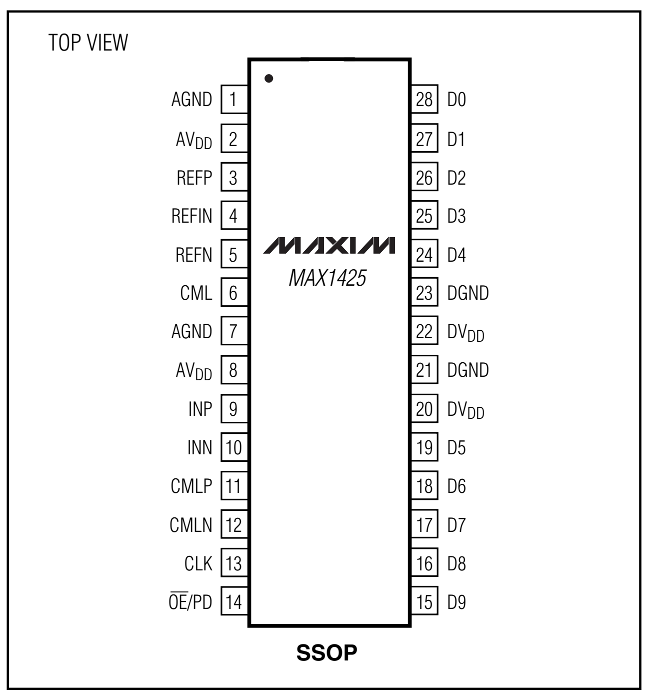
Features

- ♦ **Differential Inputs for High Common-Mode Noise Rejection**
- ♦ **Signal-to-Noise Ratio**
  61dB (at f_{IN} = 2MHz)
  59.3dB (at f_{IN} = 10MHz)
- ♦ **Internal +2.5V Reference**
- ♦ **150MHz Input Bandwidth**
- ♦ **Wide ±2V Input Range**
- ♦ **Low Power Consumption: 172mW**
- ♦ **Separate Digital Supply Input for 3V Logic Compatibility**
- ♦ **Single +5V Supply Operation Possible**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1425CAI	0°C to +70°C	28 SSOP
MAX1425EAI	-40°C to +85°C	28 SSOP

Pin Configuration



ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .... -0.3V to +6V
DV_{DD} to DGND .... -0.3V to +6V
AV_{DD} to DGND .... -0.3V to +6V
DGND to AGND .... ±0.3V
REFP, REFIN, REFN, CMLN, CMLP,
CML, INP, INN ....(V_{AGND} - 0.3V) to (V_{AVDD} + 0.3V)
CLK, $\overline{OE}$/PD, D0–D9 ....(V_{DGND} - 0.3V) to (V_{DVDD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derated 9.5mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX1425CAI .... 0°C to +70°C
MAX1425EAI.. -40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{CMLP} = +5V, V_{DVDD} = +3.3V, V_{CMLN} = V_{AGND} = V_{DGND} = 0, internal reference, digital output load = 35pF, f_{CLK} = 20MHz (50% duty cycle), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	RES			10		Bits
Differential Nonlinearity	DNL		-1		1	LSB
Integral Nonlinearity	INL		-1.5	±0.3	1.5	LSB
No Missing Codes		Guaranteed monotonic				
Midscale Offset	MSO	(Note 1)	-3	±1.0	3	%FSR
Gain Error	GE	Internal reference (Note 1)	-10	±5	10	%FSR
		External reference (REFIN) (Note 2)	-5	±2	5	%FSR
		External reference (REFP, CML, REFN) (Note 3)	-5	±3	5	
Power-Supply Rejection Ratio	PSRR	(Note 4)	-5	±2	5	mV/V
DYNAMIC PERFORMANCE (V_{INP} - V_{INN} = +2V to -2V)						
Signal-to-Noise Ratio	SNR	f = 2MHz	60	61		dB
		f = 10MHz	56	59		
Spurious-Free Dynamic Range	SFDR	f = 2MHz	70	72		dB
		f = 10MHz	64	69		
Total Harmonic Distortion (first five harmonics)	THD	f = 2MHz		-70	-67	dB
		f = 10MHz		-69	-64	
Signal-to-Noise and Distortion	SINAD	f = 2MHz	59	61		dB
		f = 10MHz	55	59		
Effective Number of Bits	ENOB	f = 2MHz	9.3	9.7		Bits
		f = 10MHz	8.8	9.5		
Intermodulation Distortion	IMD	f1 = 10.17MHz, f2 = 10.19MHz (-7dB FS, each tone) (Note 5)		-70		dBc

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{CMLP} = +5V, V_{DVDD} = +3.3V, V_{CMLN} = V_{AGND} = V_{DGND} = 0, internal reference, digital output load = 35pF, f_{CLK} = 20MHz (50% duty cycle), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT (INP, INN, CML)						
Input Resistance	R_{IN}	Either input to ground	3.5			kΩ
Input Capacitance	C_{IN}	Either input to ground		8		pF
Input Common-Mode Voltage Range	V_{CMVR}	CML (Note 6)		2.25 ±10%		V
Differential Input Range	DR	V_{INP} - V_{INN}		±2		V
Small-Signal Bandwidth	SSBW	(Note 7)		400		MHz
Large-Signal Bandwidth	LSBW	(Note 7)		150		MHz
REFERENCE (V_{REFIN} = 0; REFP, REFN, CML applied externally)						
Input Resistance	R_{IN}	REFIN (Note 8)	6.5			kΩ
Input Capacitance	C_{IN}	REFIN		10		pF
Differential Reference		V_{REFP} - V_{REFN}		2.0		V
Input Current	I_{IN}	REFP, CML, REFN	-325		325	µA
Input Capacitance	C_{IN}	REFP, CML, REFN		15		pF
REFP Input Range				3.25 ±10%		V
CML Input Range				2.25 ±10%		V
REFN Input Range				1.25 ±10%		V
REFERENCE OUTPUTS (REFP, CML, REFN; external +2.5V reference)						
Positive Reference Voltage	V_{REFP}			3.25		V
Common-Mode Reference Voltage	V_{CML}			2.25		V
Negative Reference Input Voltage	V_{REFN}			1.25		V
Differential Reference		V_{REFP} - V_{REFN}, T_A = +25°C	1.9	2.0	2.1	V
Differential Reference Temperature Coefficient				±50		ppm/°C
REFERENCE OUTPUTS (REFP, CML, REFN; internal +2.5V reference)						
Positive Reference	V_{REFP}	(Note 1)		3.25		V
Common-Mode Reference Voltage	V_{CML}	(Note 1)		2.25		V
Negative Reference	V_{REFN}	(Note 1)		1.25		V
Differential Reference		V_{REFP} - V_{REFN}, T_A = +25°C	1.8	2	2.2	V
Differential Reference Temperature Coefficient				±150		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{CMLP} = +5V, V_{DVDD} = +3.3V, V_{CMLN} = V_{AGND} = V_{DGND} = 0, internal reference, digital output load = 35pF, f_{CLK} = 20MHz (50% duty cycle), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Analog Supply Voltage	V_{AVDD}			4.75	5.00	5.25	V
Digital Supply Voltage	V_{DVDD}			2.7	3.3	5.5	V
Analog Supply Current	I_{AVDD}				31	38	mA
Analog Supply Current with Internal Reference in Shutdown		REFIN = AGND			26	35	mA
Analog Shutdown Current		$\overline{OE}$/PD = DV_{DD}			0.6	1	nA
Digital Supply Current	I_{DVDD}	V_{DVDD} = 3.3V			5.3	9	mA
		V_{DVDD} = 5.0V			8.5	14	
Digital Shutdown Current		$\overline{OE}$/PD = DV_{DD}			90	150	µA
Power Dissipation	PD				172	220	mW
DIGITAL INPUTS (CLK, $\overline{OE}$/PD)							
Input Logic High	V_{IH}	V_{DVDD} > 4.75V		2.4			V
		V_{DVDD} < 4.75V		0.7 • V_{DVDD}			
Input Logic Low	V_{IL}	V_{DVDD} > 4.75V				0.8	V
		V_{DVDD} < 4.75V				0.3 • V_{DVDD}	
Input Current Leakage		V_{DVDD} = 5.25V	I_{CLK}	-10		10	µA
			$I_{\overline{OE}/PD}$	-20		20	µA
Input Capacitance					10		pF
DIGITAL OUTPUTS (D0–D9)							
Output Logic High	VOH	I_{OH} = -200µA, V_{DVDD} = 2.7V		V_{DVDD} - 0.5		V_{DVDD}	V
Output Logic Low	VOL	I_{OL} = 200µA, V_{DVDD} = 2.7V				0.5	V
Three-State Leakage		V_{DVDD} = 5.25V, $\overline{OE}$/PD = DV_{DD}		-10		10	µA
Three-State Capacitance		$\overline{OE}$/PD = DV_{DD}			10		pF
TIMING CHARACTERISTICS							
Conversion Rate	CONV			0.1		20	MHz
Clock Frequency	f_{CLK}					20	MHz
Clock High	t_{CH}	Figure 4		20	25	30	ns
Clock Low	t_{CL}	Figure 4		20	25	30	ns
Pipeline Delay (Latency)					5.5		cycles
Aperture Delay	t_{AD}				5		ns
Aperture Jitter	t_{AJ}				7		ps
Data Output Delay	t_{OD}			5	20	25	ns
Bus Enable	t_{AD}				10	20	ns
Bus Disable	t_{AJ}				10	20	ns

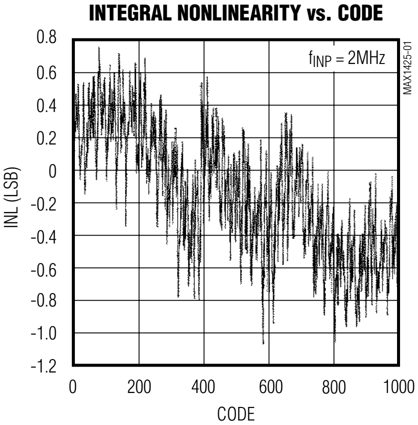
ELECTRICAL CHARACTERISTICS (continued)

Note 1: Internal reference, REFIN bypassed to AGND with a 0.1µF capacitor.
Note 2: External +2.5V reference applied to REFIN.
Note 3: Internal reference disabled. V_{REFIN} = 0, V_{REFP} = 3.25V, V_{CML} = 2.25V, and V_{REFN} = 1.25V.
Note 4: Measured as the ratio of the change in midscale offset voltage for a ±5% change in V_{AVDD} using the internal reference.
Note 5: IMD is measured with respect to either of the fundamental tones.
Note 6: Specifies the common-mode range of the differential input signal supplied to the MAX1425.
Note 7: Defined as the input frequency at which the fundamental component of the output spectrum is attenuated by 3dB.
Note 8: V_{REFIN} is internally biased to +2.5V through a 5kΩ resistor.

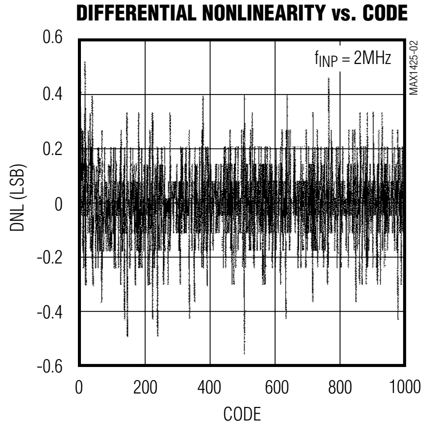
Typical Operating Characteristics

(V_{AVDD} = V_{CMLP} = +5V, V_{DVDD} = +3.3V, V_{CMLN} = V_{AGND} = 0, internal reference, digital output load = 35pF, f_{CLK} = 20Msps (50% duty cycle), for dynamic performance 0dB is full scale, T_A = +25°C, unless otherwise noted.)

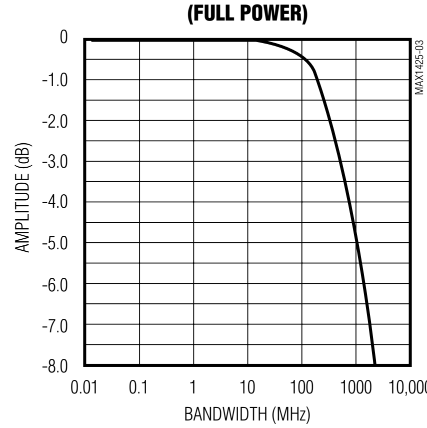
INTEGRAL NONLINEARITY vs. CODE



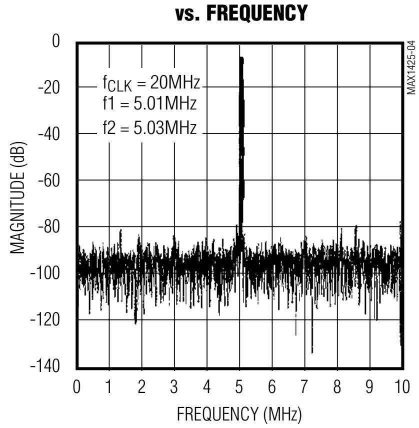
DIFFERENTIAL NONLINEARITY vs. CODE



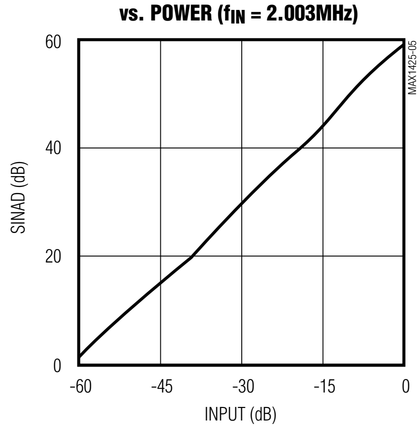
ANALOG INPUT BANDWIDTH (FULL POWER)



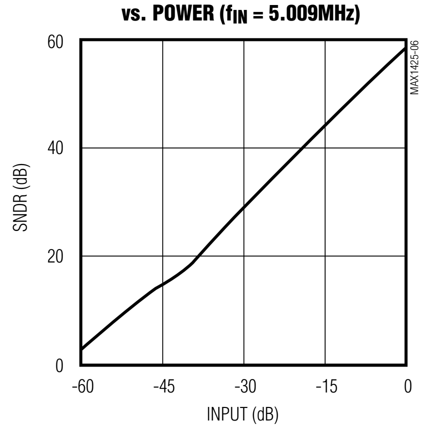
INTERMODULATION DISTORTION vs. FREQUENCY



SIGNAL-TO-NOISE PLUS DISTORTION vs. POWER (f_{IN} = 2.003MHz)



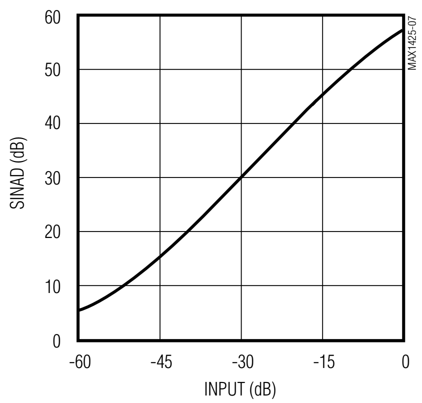
SIGNAL-TO-NOISE RATIO PLUS DISTORTION vs. POWER (f_{IN} = 5.009MHz)



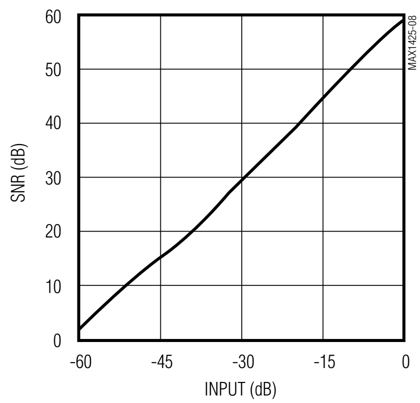
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{CMLP} = +5V, V_{DVDD} = +3.3V, V_{CMLN} = V_{AGND} = 0, internal reference, digital output load = 35pF, f_{CLK} = 20Msps (50% duty cycle), for dynamic performance 0dB is full scale, T_A = +25°C, unless otherwise noted.)

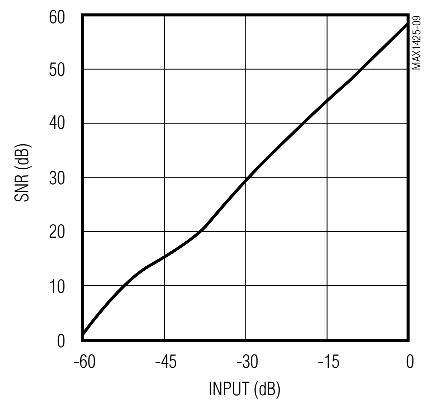
SIGNAL-TO-NOISE PLUS DISTORTION vs. POWER (f_{IN} = 9.884MHz)



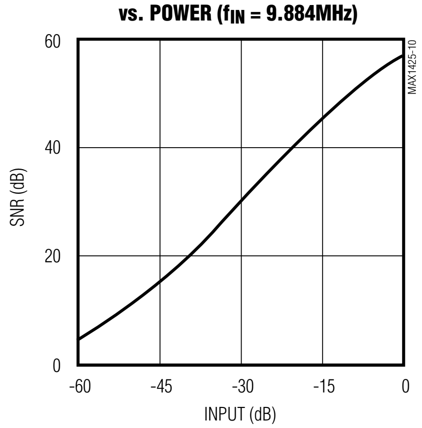
SIGNAL-TO-NOISE RATIO vs. POWER (f_{IN} = 2.003MHz)



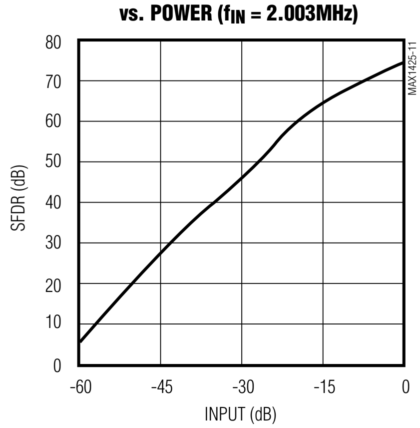
SIGNAL-TO-NOISE RATIO vs. POWER (f_{IN} = 5.009MHz)



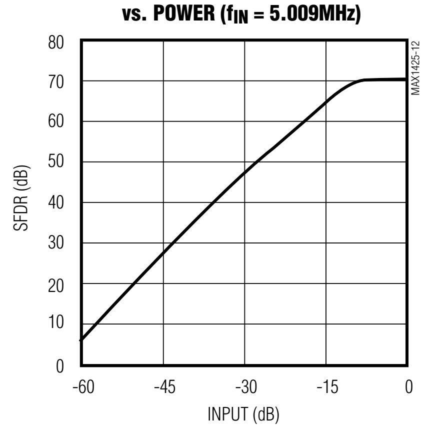
SIGNAL-TO-NOISE RATIO vs. POWER (f_{IN} = 9.884MHz)



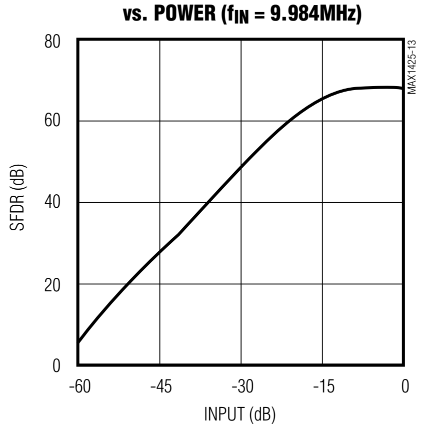
SPURIOUS-FREE DYNAMIC RANGE vs. POWER (f_{IN} = 2.003MHz)



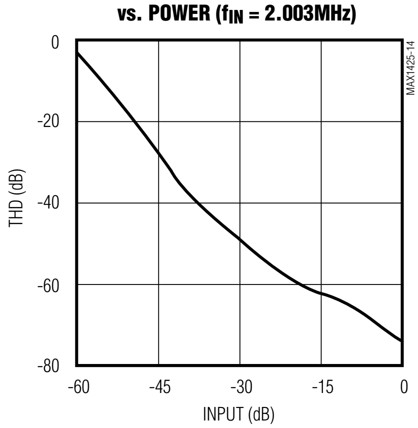
SPURIOUS-FREE DYNAMIC RANGE vs. POWER (f_{IN} = 5.009MHz)



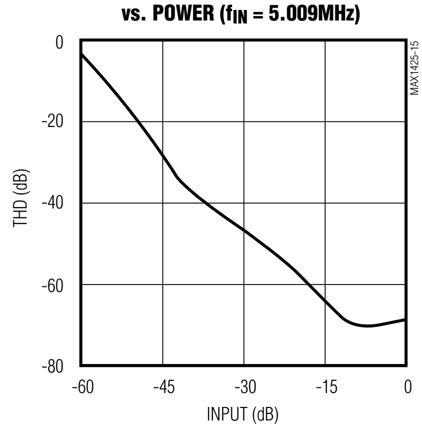
SPURIOUS-FREE DYNAMIC RANGE vs. POWER (f_{IN} = 9.984MHz)



TOTAL HARMONIC DISTORTION vs. POWER (f_{IN} = 2.003MHz)



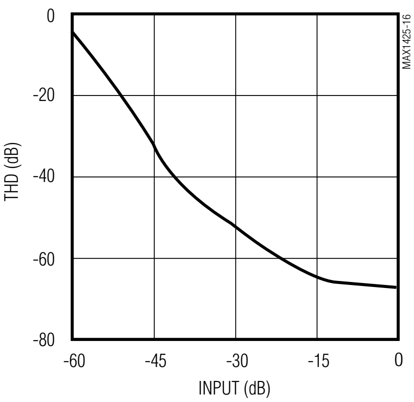
TOTAL HARMONIC DISTORTION vs. POWER (f_{IN} = 5.009MHz)



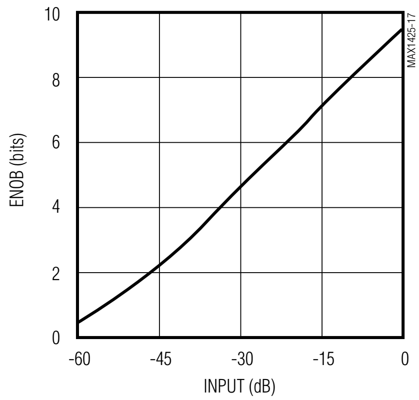
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{CMLP} = +5V, V_{DVDD} = +3.3V, V_{CMLN} = V_{AGND} = 0, internal reference, digital output load = 35pF, f_{CLK} = 20Msps (50% duty cycle), for dynamic performance 0dB is full scale, T_A = +25°C, unless otherwise noted.)

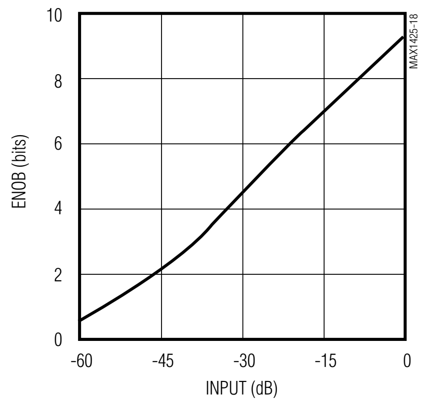
TOTAL HARMONIC DISTORTION vs. POWER (f_{IN} = 9.884MHz)



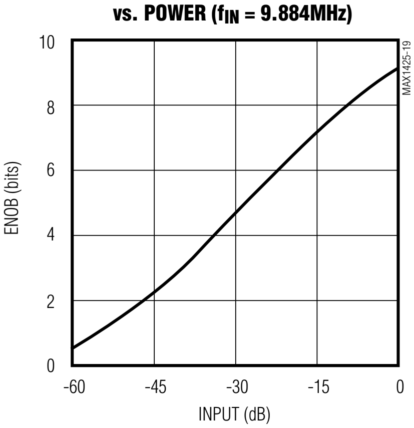
EFFECTIVE NUMBER OF BITS vs. POWER (f_{IN} = 2.003MHz)



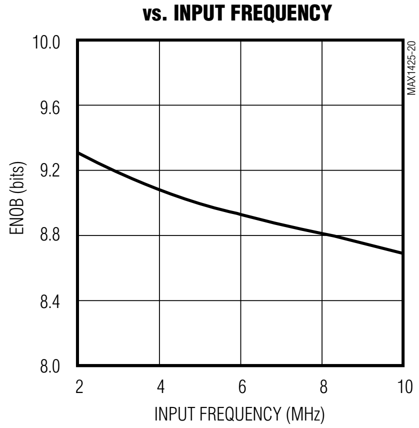
EFFECTIVE NUMBER OF BITS vs. POWER (f_{IN} = 5.009MHz)



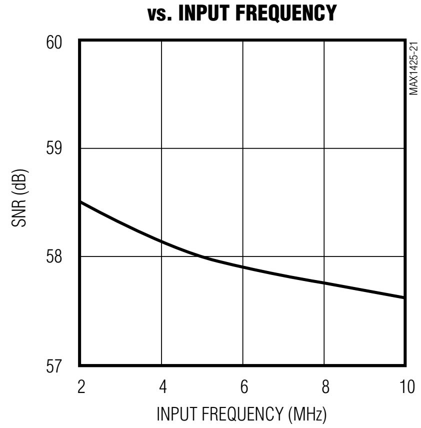
EFFECTIVE NUMBER OF BITS vs. POWER (f_{IN} = 9.884MHz)



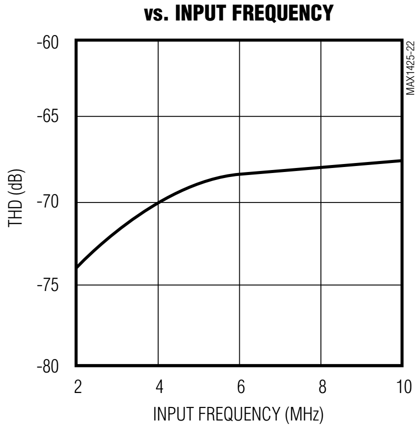
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



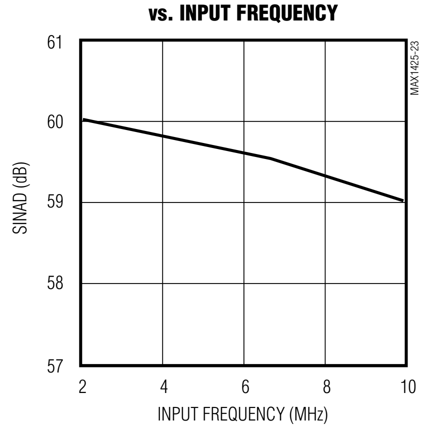
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



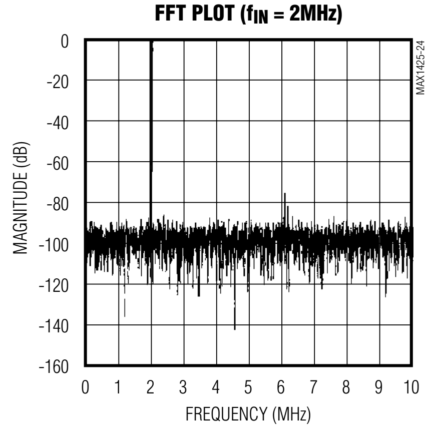
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



SIGNAL-TO-NOISE PLUS DISTORTION vs. INPUT FREQUENCY

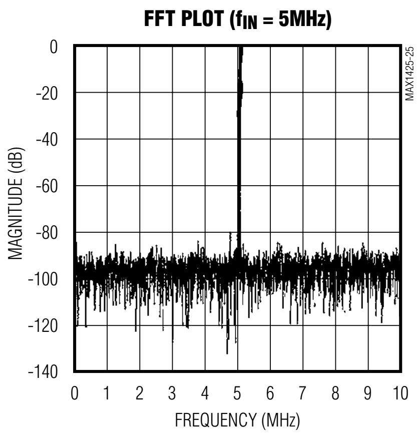


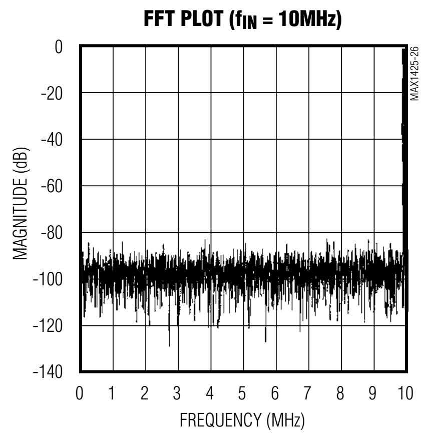
FFT PLOT (f_{IN} = 2MHz)

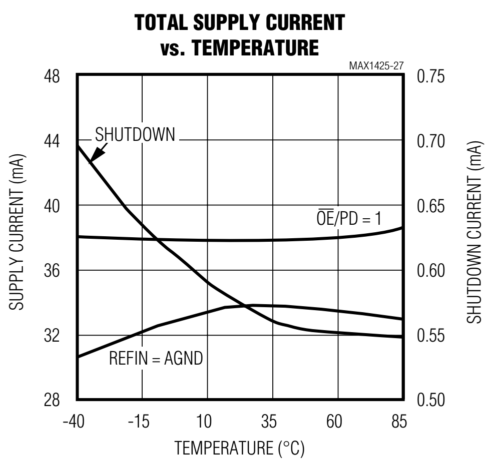


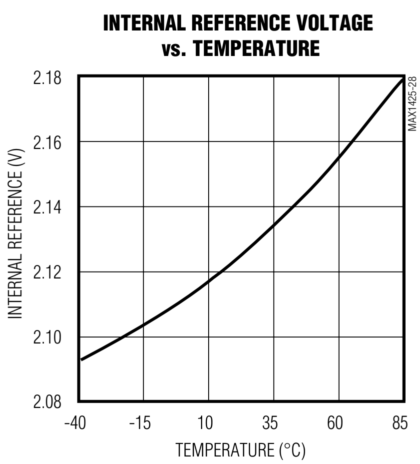
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{CMLP} = +5V, V_{DVDD} = +3.3V, V_{CMLN} = V_{AGND} = 0, internal reference, digital output load = 35pF, f_{CLK} = 20Msps (50% duty cycle), for dynamic performance 0dB is full scale, T_A = +25°C, unless otherwise noted.)









Pin Description

PIN	NAME	FUNCTION
1, 7	AGND	Analog Ground. Connect all return paths for analog signals to these pins.
2, 8	AV_{DD}	Analog Supply Voltage Input. Bypass with a parallel combination of 2.2µF, 0.1µF, and 100pF capacitors to AGND. Bypass each supply input to the closest AGND (e.g., capacitors between pins 1 and 2).
3	REFP	Positive Reference Output. Bypass to AGND with a 0.1µF capacitor. If the internal reference is disabled, REFP can accept an external voltage.
4	REFIN	External Reference Input. Bypass to AGND with a 0.1µF capacitor. REFIN can be biased externally to adjust the reference level and calibrate full-scale errors. To disable the internal reference, connect REFIN to AGND.
5	REFN	Negative Reference Output. Bypass to AGND with a 0.1µF capacitor. REFN can accept an external voltage when the internal reference is disabled (REFN = AGND).
6	CML	Common-Mode Level Input. Bypass to AGND with a 0.1µF capacitor. CML can accept an external voltage when the internal reference is disabled (REFN = AGND).
9	INP	Positive Analog Signal Input
10	INN	Negative Analog Signal Input
11	CMLP	Common-Mode Level Positive Input. For AC applications, connect to AV_{DD} to internally set the input DC bias level. For DC-coupled applications, connect to AGND.
12	CMLN	Common-Mode Level Negative Input. Connect to AGND to internally set the input DC bias level for both AC- and DC-coupled applications.
13	CLK	Clock Input. Clock frequency range from 0.1MHz to 20MHz.
14	$\overline{OE}$/PD	Active-Low Output Enable and Power-Down Input. Digital outputs become high impedance and device enters low-power mode when pin is high.
15	D9	Digital Data Output (MSB)
16–19	D8–D5	Digital Data Outputs 8–5
20, 22	DV_{DD}	Digital Supply Voltage Input. Bypass with 2.2µF and 0.1µF capacitors in parallel. Digital supply can operate with voltages as low as +2.7V.
21, 23	DGND	Digital Ground
24–27	D4–D1	Digital Data Outputs 4–1
28	D0	Digital Data Output (LSB)

Detailed Description

The MAX1425 uses a 10-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Each sample moves through a pipeline stage every half clock cycle. Counting the delay through the output latch, there is a 5.5 clock-cycle latency.

A 2-bit flash ADC converts the input voltage to digital code. A DAC converts the ADC result back into an analog voltage, which is subtracted from the held input signal. The resulting error signal is then multiplied by two, and this product is passed along to the next pipeline stage where the process is repeated. Digital error correction compensates for offsets and mismatches in each pipeline stage and ensures no missing codes.

Internal Track-and-Hold Circuit

Figure 2 shows a simplified functional diagram of the internal track-and-hold (T/H) circuit in both track mode and hold mode. The fully differential circuit samples the input signal onto the four capacitors C1a, C1b, C2a, and C2b. Switches S2a and S2b set the common mode for the amplifier input, and open before S1. When S1 opens, the input is sampled. Switches S3a and S3b then connect capacitors C1a and C1b to the output of the amplifier. Capacitors C2a and C2b are connected either to REFN, REFP, or each other, depending on the results of the flash ADC. The amplifier then multiplies the residue by two and the next stage in the pipeline performs a similar operation.

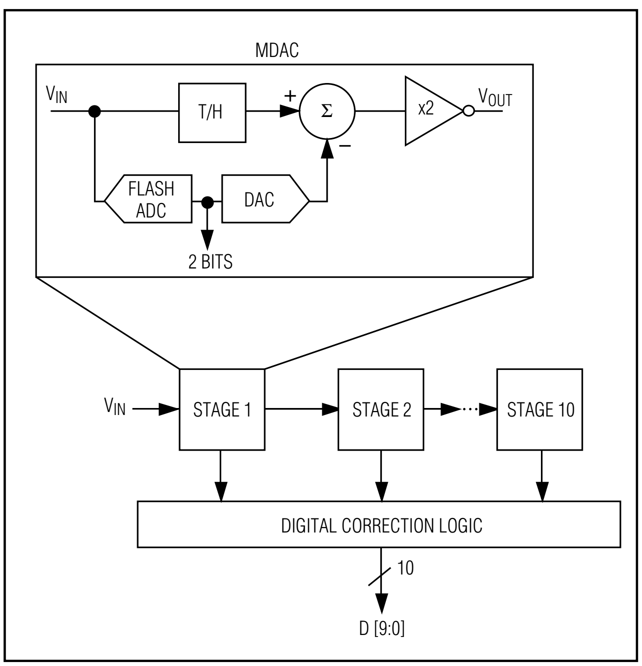


Figure 1. Pipelined A/D Architecture (Block)

System Timing Requirements

Figure 3 shows the relationship between the clock input, analog input, and data output. The MAX1425 samples the falling edge of the input clock. Output data is valid on the rising edge of the input clock. The output data has an internal latency of 5.5 clock cycles, as shown. Figure 4 shows an output timing diagram that specifies the relationship between the input clock parameters and the valid output data.

Analog Input and Internal Reference

The MAX1425 has an internal +2.5V reference used to generate three reference levels: +3.25V, +2.25V, and +1.25V corresponding to V_{REFP}, V_{CML}, and V_{REFN}. These reference voltages enable a ±2V input range. Bypass all reference voltages with a 0.1µF capacitor.

The MAX1425 allows for three modes of reference operation: an internal reference (default) mode, an externally adjusted reference mode, or a full external reference mode. The internal reference mode occurs when no voltages are applied to REFIN, REFP, CML,

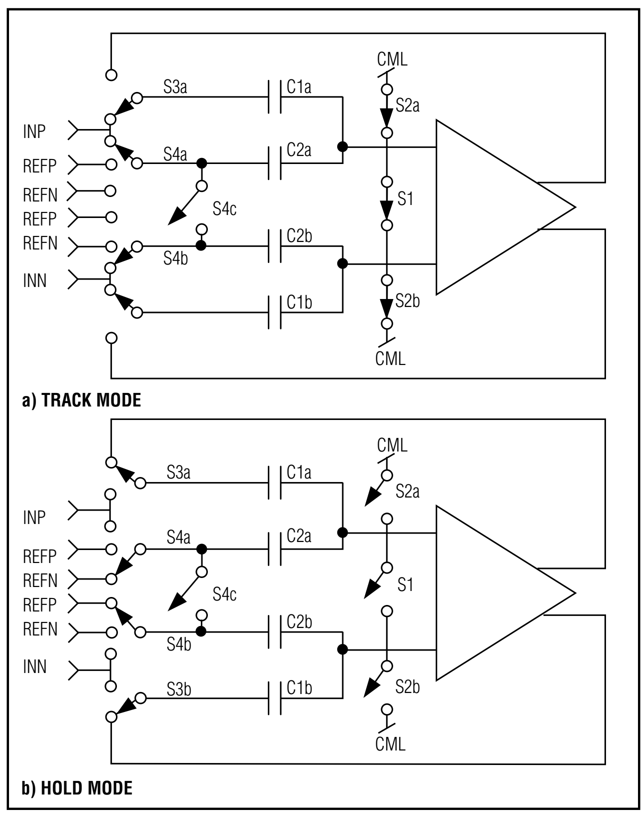


Figure 2. Internal Track-and-Hold Circuit

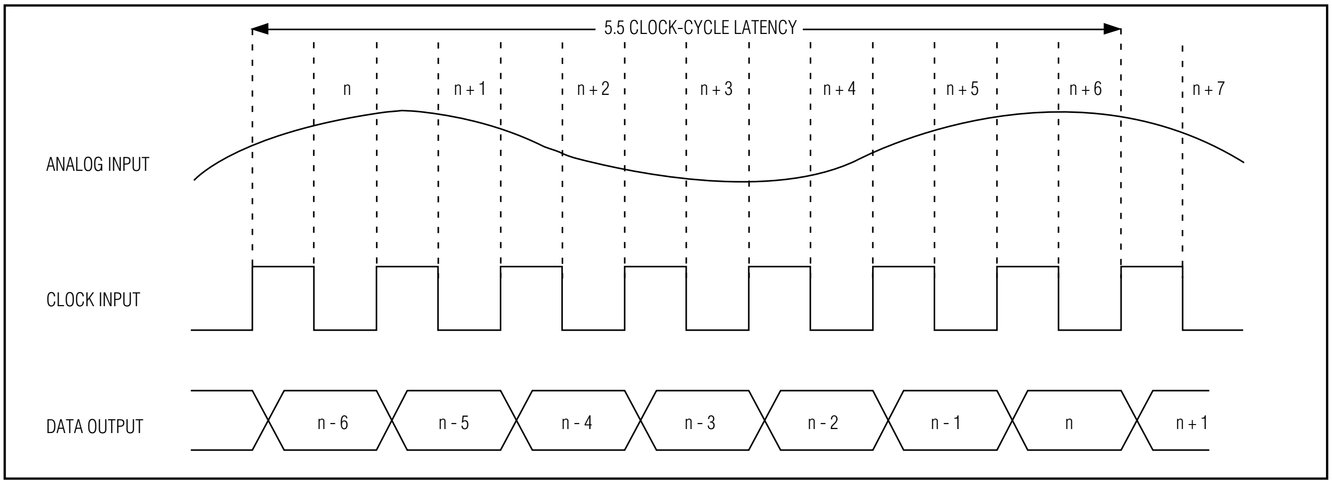


Figure 3. System Timing Diagram

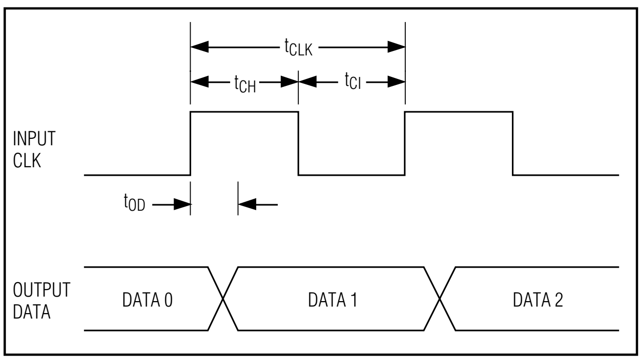


Figure 4. Output Timing Diagram

and REFN. In this mode, the voltages at these pins are set to their nominal values (see *Electrical Characteristics*). The reference voltage levels can be adjusted externally by applying a voltage at REFIN. This allows other input levels to be used as well. The full external reference mode is entered when REFIN = AGND. External voltages can be applied to REFP, CML, and REFN. In this mode, the internal reference shuts down, resulting in less overall power consumption.

Clock Input (CLK)

CLK is TTL/CMOS-compatible. Since the interstage conversion of the device depends on the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (<2ns). Low clock jitter improves SNR performance. The MAX1425 operates with a 50% duty cycle. If the clock has a duty cycle other than 50%, the clock must meet the specifications for high and low periods as stated in the *Electrical Characteristics*.

Table 1. MAX1425 Output Code

DIFFERENTIAL INPUT	OUTPUT CODE (TWO'S COMPLEMENT)
+Full Scale	0 1 1 1 1 1 1 1 1 1
+Full Scale 1LSB	0 1 1 1 1 1 1 1 1 0
+Full Scale 2LSB	0 1 1 1 1 1 1 1 0 1
+3/4 Full Scale	0 1 1 0 0 0 0 0 0 0
+1/2 Full Scale	0 1 0 0 0 0 0 0 0 0
+1/4 Full Scale	0 0 1 0 0 0 0 0 0 0
+1 LSB	0 0 0 0 0 0 0 0 0 1
Bipolar Zero	0 0 0 0 0 0 0 0 0 0
-1 LSB	1 1 1 1 1 1 1 1 1 1
-1/4 Full Scale	1 1 1 0 0 0 0 0 0 0
-1/2 Full Scale	1 1 0 0 0 0 0 0 0 0
-3/4 Full Scale	1 0 1 0 0 0 0 0 0 0
-Full Scale + 1LSB	1 0 0 0 0 0 0 0 0 1
-Full Scale	1 0 0 0 0 0 0 0 0 0

Output Enable/Power-Down Function ($\overline{OE}$/PD) and Output Data

All data outputs, D0 through D9, are TTL/CMOS-logic compatible. There is a 5.5 clock-cycle latency between the start convert signal and the valid output data. The output coding for the MAX1425 is in binary two's complement format, which has the MSB inverted (Table 1). The digital output goes into a high-impedance state and the device into a low-power mode when $\overline{OE}$/PD goes high. For normal operation, drive $\overline{OE}$ low. The outputs are not designed to drive high capacitances or

10-Bit, 20Msps ADC

heavy loads, as they are specified to deliver only 200µA for TTL compatibility. If an application needs output buffering, use 74LS74s or 74ALS541s as required.

Applications Information

Figure 5 depicts a typical application circuit containing a single-ended to differential converter. The internal reference provides a +2.25V output for level shifting. The input is buffered and then split to a voltage follower and inverter. The op amps are followed by a lowpass filter to remove some of the wideband noise associated with high-speed op amps. In this application, the amplifier outputs are directly coupled to the inputs. This configuration can also be modified for AC-coupled applications. The MAX1425 includes a DC level-shifting circuit internal to the part, allowing for AC-coupled applications. The level-shifting circuit is shown in Figure 6.

The circuit in Figure 6 can accept a 1Vp-p maximum input voltage. With a maximum clock frequency of 20MHz, use 50Ω termination to minimize reflections. Buffer the digital outputs with a low-cost, high-speed,

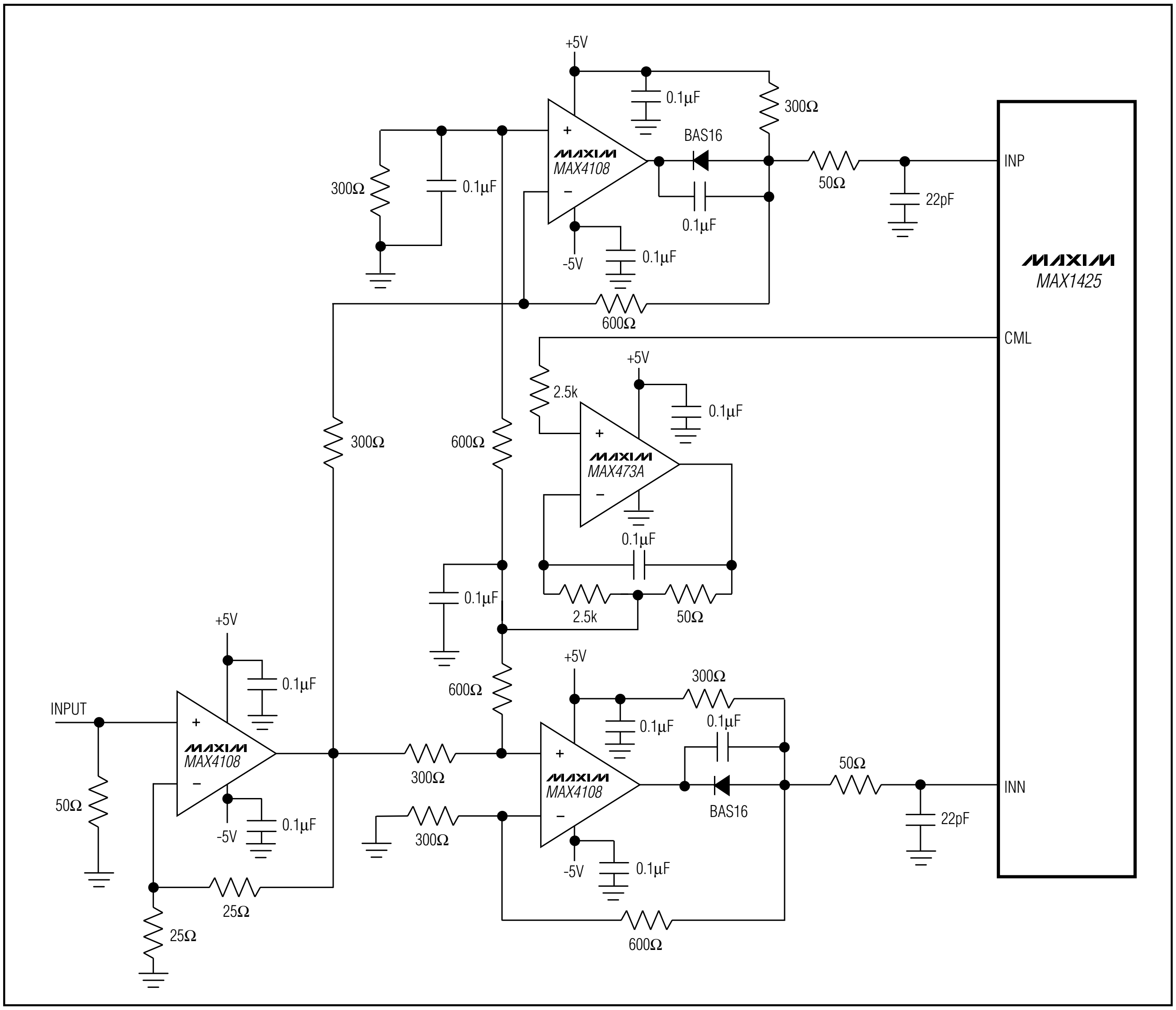


Figure 5. Typical Application Circuit Using the Internal Reference

octal D-latched flip-flop (74ALS374), or use octal buffers such as the 74ALS541.

Typical Application Using an External Reference

Figure 7 depicts an application circuit that shuts down the internal reference, allowing an external reference to be used for selecting a different common-mode voltage. This added flexibility also allows for ratiometric conversions, as well as for calibration.

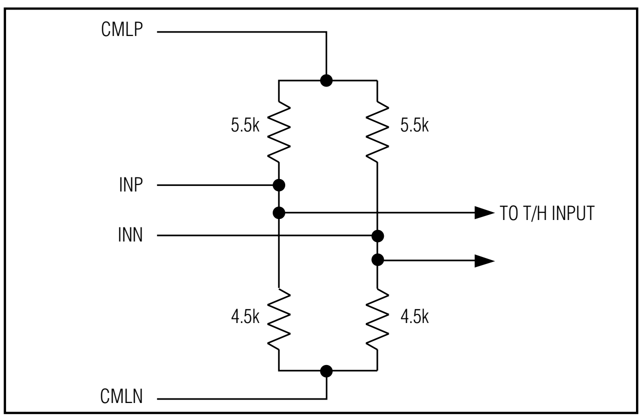


Figure 6. Analog Input DC Bias Circuit

Using Transformer Coupling

A small transformer (Figure 8) provides isolation and AC-coupling to the ADC's input. Connecting the transformer's center tap to CML provides a +2.25VDC level shift to the input. Transformer coupling reduces the need for high-speed op amps, thereby reducing cost. Although a 1:1 transformer is shown, a step-up transformer may be selected to reduce the drive requirements.

Single-Ended DC-Coupled Input Signal

Figure 9 shows an AC-coupled, single-ended application. The MAX4108 quad op amp provides high speed, high bandwidth, low noise, and low distortion to maintain the integrity of the input signal.

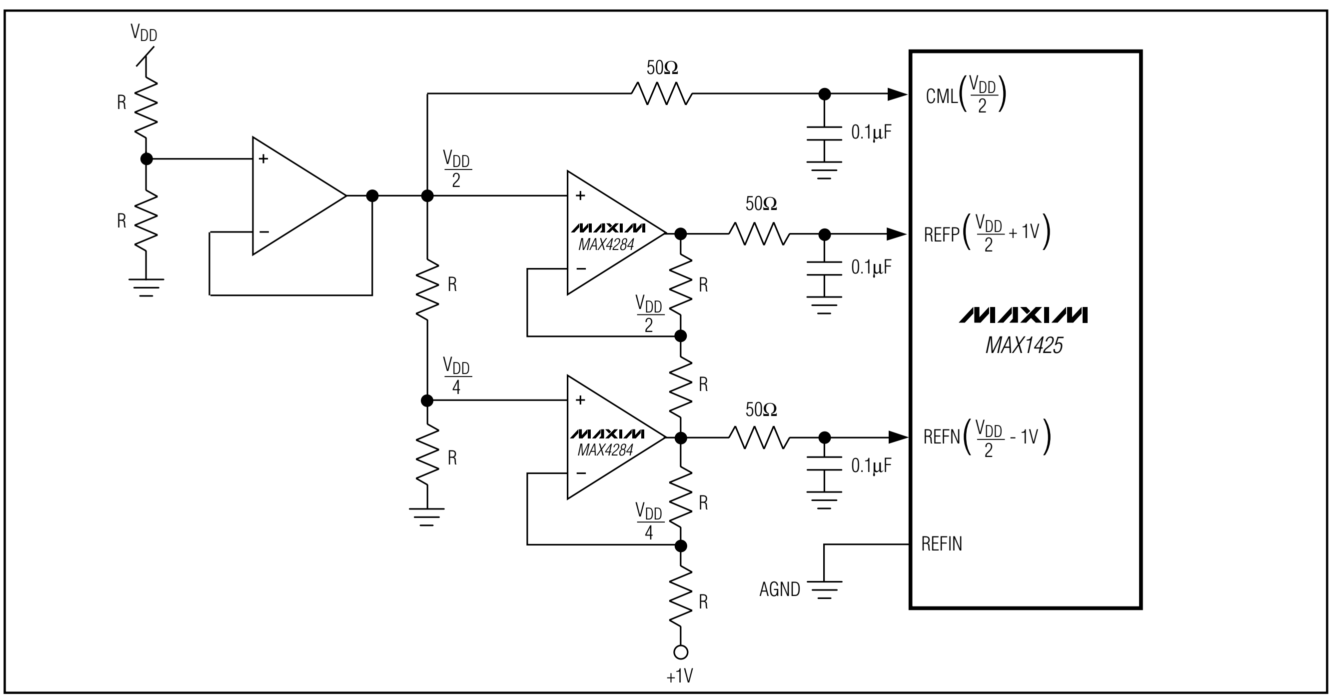


Figure 7. Using an External Reference for REFP, REFN, and CML (internal reference shut down)

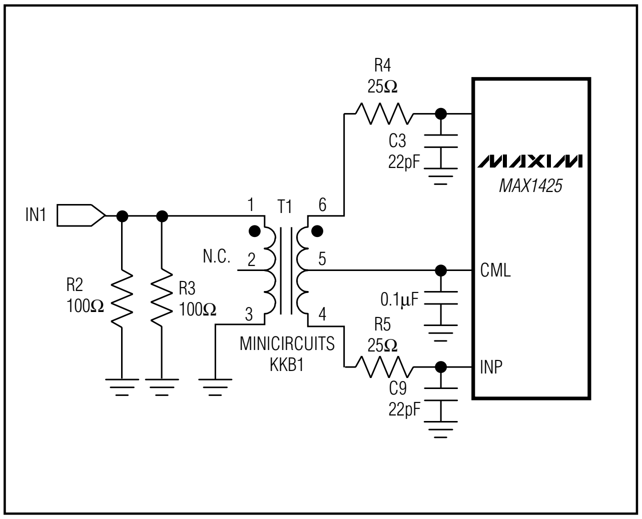


Figure 8. Using a Transformer for AC-Coupling

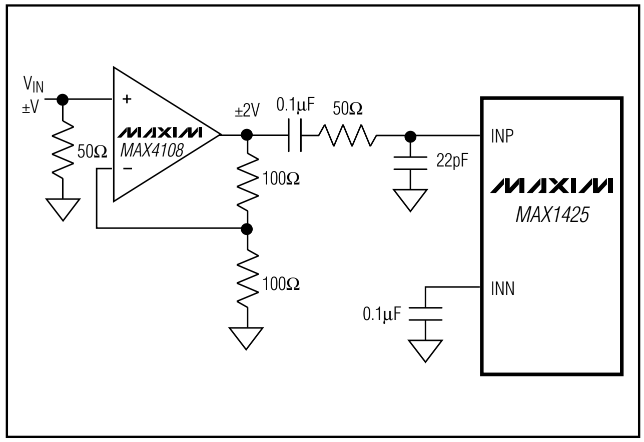


Figure 9. Single-Ended AC-Coupled Input Signal

Bypassing and Board Layout

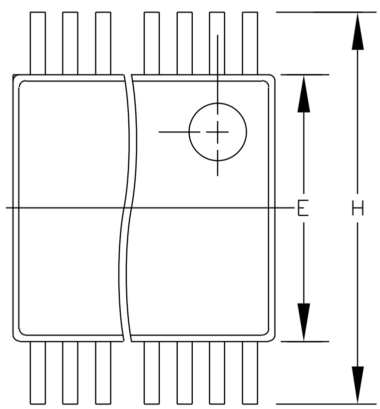
The MAX1425 requires high-speed board layout design techniques. Locate all bypass capacitors as close to the device as possible, using surface-mount devices for minimum inductance. Bypass all analog voltages (AV_{DD}, REFIN, REFP, REFN, and CML) to AGND. Bypass the digital supply (DV_{DD}) to DGND. Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Route high-speed digital signal traces away from sensitive analog traces. Matching impedance, especially for the input clock generator, may reduce reflections, thus providing less jitter in the system. For optimum results, use low-distortion complementary components such as the MAX4108.

Chip Information

TRANSISTOR COUNT: 5305

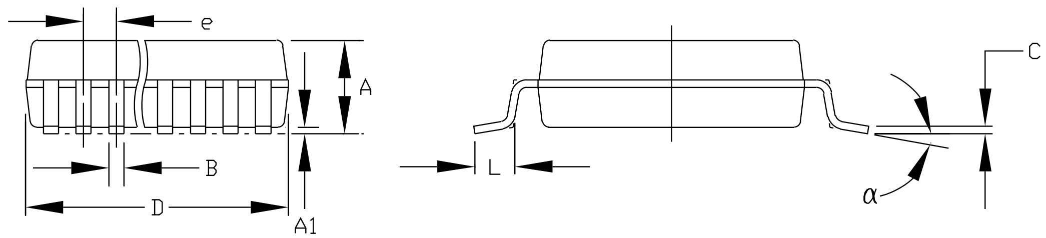
Package Information

SSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, SSOP, 5.3X.65mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0056	A	1/1

NOTES